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A 177 ppm RMS Error-Integrated Interface for Time-Based Impedance Spectroscopy of Sensors

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Abstract: This paper presents an integrated circuit for time-based electrical impedance spectroscopy (EIS) of sensors. The circuit exploits maximum-length sequences (MLS) in order to perform a broadband excitation of the sensors under test. Therefore, the measured time-domain EIS is obtained by cross-correlating the input with the output of the analog front end (AFE). Unlike the conventional digital approach, the cross-correlation operation is performed in the analog domain. This leads to a lower RMS error in the measured time-domain EIS since the signal processing is not affected by the quantization noise of the analog-to-digital converter (ADC). It also relaxes the sampling frequency of the ADC leading, along with the lack of random access memory (RAM) usage, to a reduced circuit complexity. Theoretical concepts about the circuit's design and operation are presented, with an emphasis on the thermal noise phenomenon. The simulated performances are shown by testing a sensor's equivalent model composed of a 50 kΩ resistor in parallel with a 100 pF capacitor. A time-based EIS output of 255 points was obtained with a maximum tested frequency of 500 kHz and a simulated RMS error of 0.0177% (or 177 ppm).

Keywords: EIS; MLS; CMOS; impulse response; cross-correlation

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1. Introduction

Impedance analysis instrumentation plays an important role in material development and characterization, biological research, and sensors' read-outs. It is a valuable tool for investigating the electrical and physical parameters of matter and is also used to enhance the read-out performance in sensing applications [1]. Some examples of applications of impedance analysis are bioelectrical impedance (BioZ) measurement [2], electrical assessment of the cell metabolism [1], online built-in test for DC–DC converters [3], estimation of battery parameters due to aging [4], etc. In recent years, a plethora of electronic solutions for impedance analysis, both discrete component and integrated, have been presented [5] in order to accomplish the variety of requirements needed by the applications. Compared to discrete-component solutions, integrated circuits offer the advantage of overcoming the common accuracy issues of laboratory instrumentation [6]. Moreover, integrated solutions allow for the realization of miniaturized and portable analyzers, which are suitable for modern Internet-of-Things or point-of-care devices [5,7].

The most commonly implemented approach is synchronous detection (SD) [8], which consists of (1) a voltage-controlled current source (VCCS) for the stimulus injection between a pair of electrodes; (2) an instrumentation amplifier (IA) for signal preamplification; and (3) two multipliers for the extraction of the real parts (in-phase demodulation) and imaginary parts (quadrature demodulation) from the measured signal. This approach suffers from matching, offset, and synchronization issues between the stimulus and measuring subcircuits [6]. As an alternative, a self-mixing full-wave rectifier was used in [9]

to implement a polar demodulation method. The magnitude and phase information were extracted, giving a simulated magnitude error of 0.3% with a max tested frequency of 1 MHz. Information on the magnitude and phase of the impedance was also obtained through the system presented in [6] with a similar approach. The achieved measured error on the magnitude was 1.15% with a maximum tested frequency of 100 kHz. In [10], an alternative approach based on $\Delta\Sigma$ demodulation was implemented achieving 15 bits of resolution and high temperature accuracy with a maximum working frequency of 16 kHz. All these systems rely on single-tone sinusoids in order to perform the measurements, which exhibit the following drawback: the total measurement time resulting from the evaluation of multiple frequencies is the sum of the measurement times for each frequency. Moreover, the total time is limited by the minimum frequency used for the excitation.

Unlike sinusoids, which are narrow-band excitation signals, broadband signals can be used to stimulate the impedance under test in a wide frequency range while keeping a low total measurement time [2]. Popular signals used for broadband excitation are maximum-length sequences (MLS). These are pseudo-random binary signals with unique mathematical properties, thanks to which the impedance measurement can be performed in the time domain, requiring only the digital cross-correlation as a processing algorithm [5,11]. As an example, in [6] an MLS-based measurement circuit for bio-impedance spectroscopy was implemented. The system was able to measure 63 points (sixth-order MLS) with a maximum tested frequency of 125 kHz, achieving a modest error performance of greater than 10% for the absolute resistor values.

In this paper, an integrated circuit for time-based impedance spectroscopy of sensors is presented. The circuit uses MLS-based signals for impedance analysis but unlike the conventional approach with digital cross-correlation, the signal processing is performed through analog circuits. Since the ADC is moved after the processing, the cross-correlation result is not affected by quantization noise but only by electronic noise.

This paper is organized as follows. Section 2 presents an overview of the proposed analog approach for time-based EIS measurement. Section 3 deals with the circuit design of the system. A first-order equivalent circuit is considered for the sensor's electrical model. Details about the noise performance are given through mathematical analysis. Section 4 shows the simulation results from the SPECTRE simulator and Cadence Virtuoso platform, which validate the circuit's operation. Finally, the obtained parameters from the simulation are compared with state-of-the-art works.

2. System Architecture

2.1. Overview and Conventional Approach

MLS-based signals are used as broadband excitation signals for sensors under test (SUT). These signals are a subclass of pseudo-random binary sequences (PRBS) and are generated through simple digital circuits called linear feedback shift registers (LFSR). Given L is the order of a generic LFSR, it generates an MLS of $N = 2^L - 1$ binary symbols. LFSR circuits find countless applications in information theory, one of which is the measurement of the impulse response (IR) of linear and time-invariant (LTI) systems. Let $m[n]$ be the MLS input of an LTI system, $y[n]$ its output array, and $h[n]$ its IR. The latter can be measured by cross-correlating the input array, m, with the output array, y, as follows [5,12]:

$$\Phi_{my}[n] = m[n] \star y[n] = \frac{1}{N} \sum_{j=0}^{N-1} m[i-n] \cdot y[i] = \Phi_{mm}[n] * h[n] \approxeq h[n] \quad (1)$$

where the $[i-n]$ index is evaluated by modulo N, $\star$ denotes the circular cross-correlation operation, Φ_{mm} is the circular auto-correlation of the m sequence, and $*$ denotes the convolution operator. Since for high N values $\Phi_{mm}[n]$ approximates the Kronecker delta function, $\delta[n]$, the approximate result of the circular cross-correlation between $\Phi_{mm}[n]$ and $h[n]$ is actually $h[n]$.

This principle is implemented by the conventional architecture shown in Figure 1. The system consists of an LFSR that generates the $V_m[n]$ input signal for the AFE, which embeds the SUT. The clock signal of the LFSR has a frequency equal to f_m. The AFE output, $V_y(t)$, is sampled from the ADC with a sampling rate equal to f_s. Thus, the digital cross-correlation operation is carried out, taking the $V_m[n]$ input and the $V_y[n]$ output as operators. Finally, the Φ_{my} system output is approximately equal to the IR of the composite system formed by the AFE and the sensor. The conventional architecture seen in Figure 1 exhibits a drawback concerning the error in the measured IR. This error comes from the electronic noise of the AFE and to a greater extent from the quantization noise of the ADC, which must have a high resolution in order to increase the signal-to-noise ratio (SNR) of the measured IR [5]. Moreover, the sampling rate of the ADC must be greater than or equal to the MLS frequency in order to convert enough samples for the cross-correlation operation.

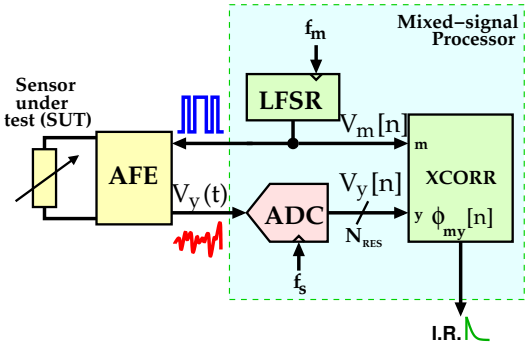

Figure 1. Conventional architecture for MLS-based EIS of sensors.

As a novelty with respect to state-of-the-art features, the proposed circuit aims to increase the SNR of the measured IR by realizing the cross-correlation operation through an analog circuit. The analog-to-digital conversion is moved after the signal processing. This solution exhibits the following key advantages:

- The quantization noise no longer affects the cross-correlation operation; thus, only the electronic noise contributes to the error in the measured IR;
- Since the ADC must convert only the last sample of the entire cross-correlation process, the sampling rate requirement of the ADC is greatly relaxed;
- RAM usage is totally avoided, simplifying the digital design of the system.

2.2. Proposed Analog Solution

The aforementioned principle of IR measurement is adopted here to measure the discrete-time inverse Laplace transform of a generic sensor's impedance, henceforth referred to as $Z_s(s)$. Figure 2 depicts the proposed analog solution. The system consists of three main blocks:

- **Digital Control Unit (DCU):** This unit generates two MLS sequences, namely **m** and $\mathbf{m}_i$, expressed here as arrays. More specifically, **m** is a standard MLS, whereas $\mathbf{m}_i$ replicates **m** with an i start index that is incremented at every completion of **m**. The clock frequency of the DCU is the same as that of the MLS, i.e., f_m. The M number of binary symbols is selected by the user through the M_SEL configuration word. The DCU is also responsible for the generation of the SAMPLE_RDY and XC_END control signals;
- **AFE (analog front end):** This is a charge pump-based front-end circuit for the SUT. It drives the sensor with a pseudo-random binary current signal of $\pm I_m$ amplitude. This current signal is generated from the **m** sequence. The output of the AFE is the voltage across the sensor in response to the binary current;
- **Switched-Capacitor Integrator:** This integrates the $V_o(t)$ voltage into the discrete time. Its clock signal is provided through the INT_CLK input port and it has the same clock frequency as the MLS, i.e., f_m. The integrator has the option to change the gain of

the integration through the S configuration word. Moreover, the sign of the integration can be changed through the SGN binary input. This feature is essential in order to properly implement the cross-correlation operation in an analog fashion. Regarding the HOLD input, when set to 1, the integrator stops its operation while maintaining the stored value. The integrator's output voltage, $V_\Phi[n]$, is the output of the system and it is sampled by an external ADC at a lower sample rate as the SAMPLE_RDY signal goes higher.

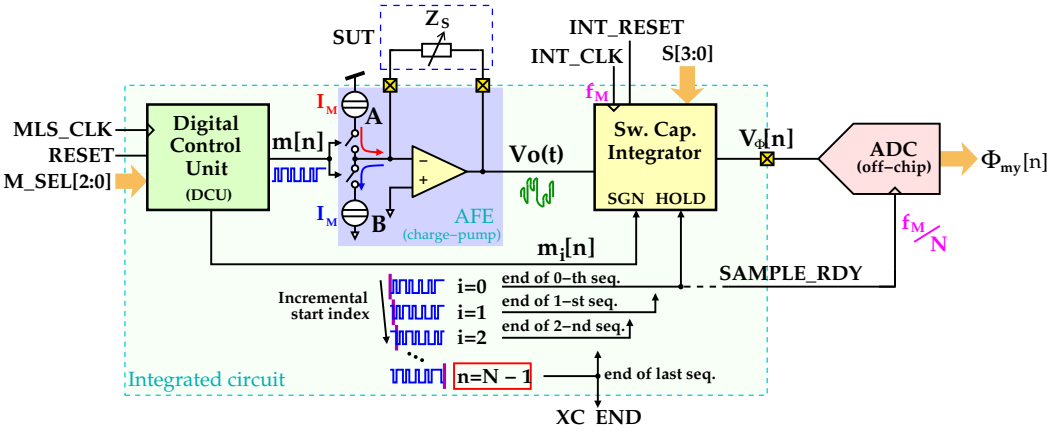

Figure 2. System architecture of the proposed integrated analog and mixed-signal solution.

As mentioned before, $\mathbf{m}_i$ is a circularly shifted replica of $\mathbf{m}$, with i being the start index that is incremented at every sequence completion. As the RESET signal (active high) returns to 0, the system starts its operation and the DCU starts generating the $\mathbf{m}$ and $\mathbf{m}_i$ sequences. The MLS array is expressed as follows:

$$\boldsymbol{m} = [b_0, b_1, b_2, \ldots, b_{N-1}] \tag{2}$$

where the terms in $\mathbf{m}$ are binary symbols with values equal to ± 1. The $N \times N$ MLS circulant matrix, formed by the shifted $\mathbf{m}$ sequences, is expressed as follows:

$$\boldsymbol{C} = \begin{bmatrix} b_0 & b_1 & \ldots & \ldots & b_{N-2} & b_{N-1} \\ b_1 & b_2 & & & b_{N-1} & b_0 \\ \vdots & & \ddots & & & \vdots \\ \vdots & & & \ddots & & \vdots \\ b_{N-2} & b_{N-1} & & & b_{N-4} & b_{N-3} \\ b_{N-1} & b_0 & \ldots & \ldots & b_{N-3} & b_{N-2} \end{bmatrix} = \begin{bmatrix} \boldsymbol{m_0} \\ \boldsymbol{m_1} \\ \vdots \\ \vdots \\ \boldsymbol{m_{N-2}} \\ \boldsymbol{m_{N-1}} \end{bmatrix} \tag{3}$$

With reference to Figure 2, the discrete-time $V_o[n]$ voltage sampled with a sampling period of $T_s = 1/f_m$ is expressed as follows:

$$V_o[n] \approxeq T_S \cdot \left[\mathcal{L}^{-1}\{-|I_m| \cdot Z_s(s)\} \right] \Big|_{t=n \cdot T_S} \tag{4}$$

where the T_S scaling factor comes from the discrete-to-continuous time conversion performed by the AFE circuit. The latter acts as a 1-bit digital-to-analog converter (DAC) followed by a sample and hold. This operation, which can be described by a zero-order hold (ZOH) mathematical model, is not a perfect digital-to-analog conversion [13] and this is the reason for the approximately equal sign in (4). The values of (4) are expressed as an N-sample array as follows:

$$\mathbf{V_o} = [V_{o,0}, V_{o,1}, V_{o,2}, \ldots, V_{o,N-1}] \tag{5}$$

The discretized time-domain impedance, i.e., the inverse Laplace transform of the $Z_s(s)$ sensor's impedance, is given by cross-correlating the $V_o[n]$ output voltage with $m[n]$. This is accomplished through the integrator, whose integration's sign selection implements the multiplication between the analog voltage and the MLS sequence. Indeed, the latter only includes binary values equal to ± 1. The integrator's output voltage, $V_\Phi[n]$, has the following expression in the discrete-time domain:

$$V_\Phi[n] = \Gamma \cdot \sum_{i=0}^{N-1} m[i-n] \cdot V_o[i] \tag{6}$$

where Γ is the integrator's gain. By substituting (4) in (6) and thanks to (1), the following equation is obtained:

$$V_\Phi[n] \cong -T_S \cdot \Gamma \cdot N \cdot |I_m| \cdot \Phi_{mm}[n] * \left[\mathcal{L}^{-1}\{Z_s(s)\}\right]\Big|_{t=n\cdot T_S} \tag{7}$$

where $\Phi_{mm}[n]$ is the circular auto-correlation of the $m[n]$ sequence and $*$ denotes the convolution operator. The discrete-time impedance appears in (7) instead of the impulse response since the input and the output of the SUT are a current and a voltage, respectively. The $\mathbf{V_\Phi}$ array, comprising the sampled values of the integrator's output, is defined as follows:

$$\mathbf{V_\Phi} = [V_{\Phi,0}, V_{\Phi,1}, V_{\Phi,2}, \ldots, V_{\Phi,N-1}] \tag{8}$$

The approximated expression of the discretized time-domain impedance of the sensor is obtained from the integrator's voltage, $V_\Phi[n]$, as follows:

$$\frac{V_\Phi[n]}{\psi} \cong -\left[\mathcal{L}^{-1}\{Z_s(s)\}\right]\Big|_{t=n\cdot T_S} \tag{9}$$

where ψ is a scaling factor and is equal to $T_S \cdot \Gamma \cdot N \cdot |I_m|$. Equation (6) can be expressed in compact form using matrix multiplication. Thus, the $\mathbf{C}$ circulant matrix generated from the DCU and expressed in (3) is introduced:

$$\mathbf{V_\Phi} = \Gamma \cdot (\boldsymbol{C}\, \boldsymbol{V_o}) \tag{10}$$

Following the approach developed for (9), the same result in matrix form is obtained:

$$\frac{\mathbf{V_\Phi}}{\psi} = -\boldsymbol{h_z} \cong -\begin{bmatrix} \left[\mathcal{L}^{-1}\{Z_s(s)\}\right]\Big|_{t=0} \\ \left[\mathcal{L}^{-1}\{Z_s(s)\}\right]\Big|_{t=T_S} \\ \vdots \\ \vdots \\ \left[\mathcal{L}^{-1}\{Z_s(s)\}\right]\Big|_{t=(N-2)\cdot T_S} \\ \left[\mathcal{L}^{-1}\{Z_s(s)\}\right]\Big|_{t=(N-1)\cdot T_S} \end{bmatrix} \tag{11}$$

Besides the aforementioned advantages, the solution also exhibits a drawback concerning an increase in the measurement time. This is the amount of time needed to perform the entire cross-correlation operation and it can be derived as follows:

$$t_{meas} = \frac{N \cdot (N+1)}{f_m} \tag{12}$$

Comparing the t_{meas} with that in the conventional approach of [5], it turns out that the measurement time required by the analog approach is $N+1$ times greater than the conventional approach.

3. Circuit Design

3.1. Analog Front End (AFE)

Figure 3 shows the circuit schematic of the AFE.

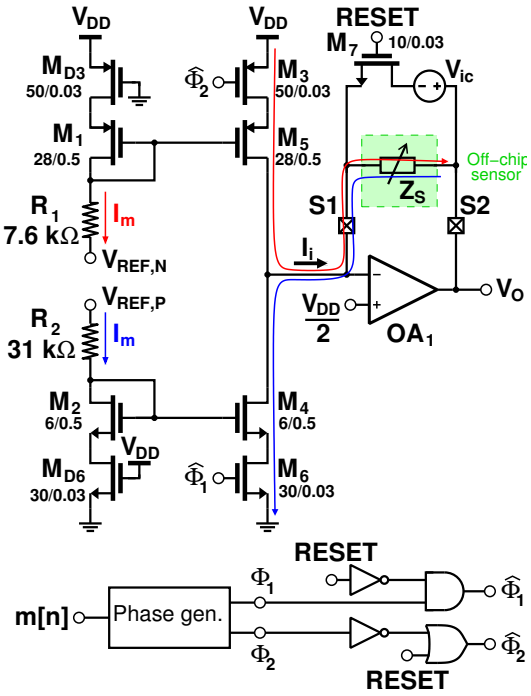

Figure 3. Circuit schematic of the implemented AFE. The specified width/length are reported in µm for each MOSFET.

The circuit is based on a charge-pump architecture. The voltages $V_{REF,P}$ and $V_{REF,N}$ are provided by an external voltage source, which set them at 800 mV and 100 mV, respectively. These voltages were chosen to obtain the same current value, $|I_m|$, equal to 10 µA for both branches. The currents are then mirrored by $M_1 - M_5$ and $M_2 - M_4$ current mirrors. M_{D3} and M_{D6} are dummy transistors and they are always in an on state with the aim of equalizing the drain-source voltages, V_{DS}, of the M_3 and M_6 switches in order to increase the accuracy of the mirrored currents. The Z_s sensor is connected between the pads S1 and S2. The gate terminals of the M3 and M6 switches are driven by $\widehat{\Phi_1}$ and $\widehat{\Phi_2}$ signals, which are generated by a non-overlapping phase generator starting from the **m** sequence. The M7 switch is driven by the RESET signal and it is turned on at every sequence completion. Its aim is to force the Z_S terminals at a $V_{DD}/2 + V_{ic}$ voltage. V_{ic} represents the sensor's initial condition and it is pre-computed by a MATLAB simulation. Since an approximate value of V_{ic} is used in the results in Section 4, an error in the cross-correlation operation is expected from the simulations.

As for the implementation of the OA1 opamp, a two-stage Miller architecture was adopted, as depicted in Figure 4. The simulated specifications of the frequency response in a typical corner are reported in Table 1.

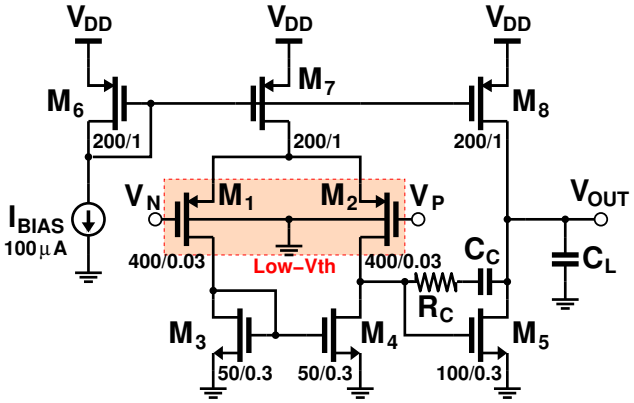

Figure 4. Circuit schematic of the implemented opamp for the sensor driver. The specified width/length are reported in µm for each MOSFET.

Table 1. Specifications of the designed opamp obtained through circuit simulations.

Parameter	Value
DC Gain	60 dB
Gain-Bandwidth Product (GBW)	105 MHz
Phase Margin (PM)	53 Deg

The differential pair made up of the M_1 and M_2 MOSFETs was designed using low-threshold voltage (LVT) devices offered by the adopted FD-SOI technology. The sizing criterion for the opamp specifications in terms of the gain and GBW (henceforth called ω_T) is detailed as follows. By assuming a dominant pole model for the opamp having A_0 gain and ω_B pole, the approximated transfer function from the $I_i(s)$ input current to the $V_o(s)$ output voltage of the AFE in Figure 3 can be derived as follows:

$$H_z(s) = \frac{V_o(s)}{I_i(s)} \approxeq -\frac{R_s}{s \cdot \left(\frac{1}{\omega_S} + \frac{1}{\omega_T}\right) + 1} = -\frac{R_s}{s \cdot (\tau + \Delta\tau) + 1} \tag{13}$$

where ω_T is the $A_0 \cdot \omega_B$ product, $\omega_S = 1/\tau$ is the sensor's pole equal to $1/(R_S \cdot C_S)$, and $\Delta\tau = 1/\omega_T$ is the error in the measured sensor's constant time due to the finite gain and bandwidth of the opamp. The relative error can be derived as follows:

$$\epsilon_\tau = \frac{\Delta\tau}{\tau} = \frac{1}{R_S \cdot C_S \cdot \omega_T} \tag{14}$$

The desired error depends on the application and the sensor. As an application example, the case of impedance spectroscopy of a metal-oxide (MOX) gas sensor could be considered for the ω_T sizing. These sensors exhibit a typical parasitic capacitance, C_S, of about 1 pF and a wide resistance value, R_S, from a few kΩ to several MΩ [14]. For instance, assuming a typical resistance value of 160 kΩ, in order to achieve an error of 1% on the measured τ [5], it turns out from (14) that an opamp with a ω_T greater than 100 MHz is needed.

3.2. Switched-Capacitor Integrator

Figure 5 shows the adopted circuit schematic of the switched-capacitor integrator. The chosen architecture can be found in [15–17] and resembles the classical schematic of a stray insensitive integrator. The circuit employs the correlated double-sampling (CDS) technique in order to remove the effects of both the offset voltage and the flicker noise of the OA1 opamp. Similar to the sensor driver, the common-mode voltage, V_{cm}, was set to $V_{DD}/2$, which is 500 mV. The generator V_{OS} in the schematic represents the offset contribution of the opamp. The C_F feedback capacitor assumes discrete values according to the S configuration word. By changing this, the user changes the integration gain, Γ, depending

on the application and the sensor's dynamic behavior. The sign of the integration, which is useful for the accomplishment of the multiplication by the **m** binary samples, is changed by swapping the clock phases of the M1 and M2 MOSFETs. In particular, as Φ_A coincides with Φ_1 and Φ_B coincides with Φ_2, the integration sign is negative. On the contrary, as Φ_A coincides with Φ_2 and Φ_B coincides with Φ_1, the integration sign is positive. The $C_{S,2}$ auxiliary capacitor stores the V_{OS} offset voltage and the input-referred flicker noise contributions of the opamp during the sampling operation (M1, M3, M4, M6 in an on state). These contributions are subtracted from the integrated value during the integration operation (M2, M5 in an on state). The same opamp as in Figure 4 was used for the OA1 implementation.

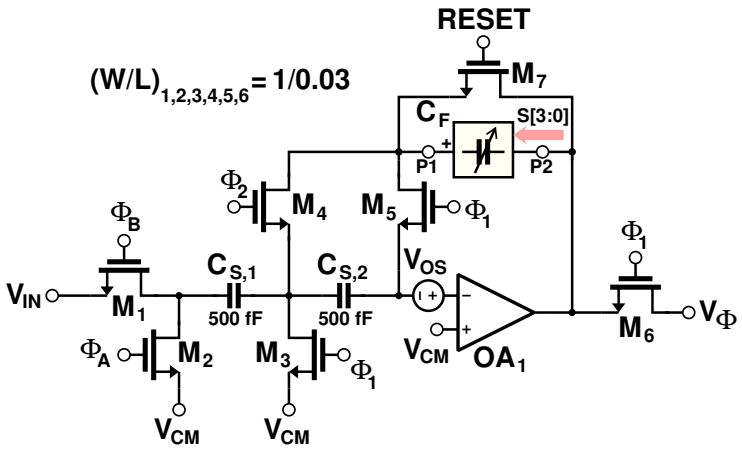

Figure 5. Circuit schematic of the implemented switched-capacitor integrator. The specified width/length are reported in µm for each MOSFET.

The phase-swapping operation is performed using the digital circuit depicted in Figure 6. The Φ_A and Φ_B signals are generated starting from the INT_CLK clock signal with a frequency equal to f_m. With reference to the upper circuit in Figure 6, the INT_CLK clock and its inverted replica are swapped through two multiplexers. Thus, as the SGN signal assumes a high value, Φ_A coincides with Φ_1 and Φ_B coincides with Φ_2. As the SGN assumes a low value, Φ_A is equal to Φ_2 and Φ_B is equal to Φ_B.

The choice of the f_m sampling frequency for the discrete-time integrator also limits the max detectable bandwidth of the system for the SUT to $f_m/2$.

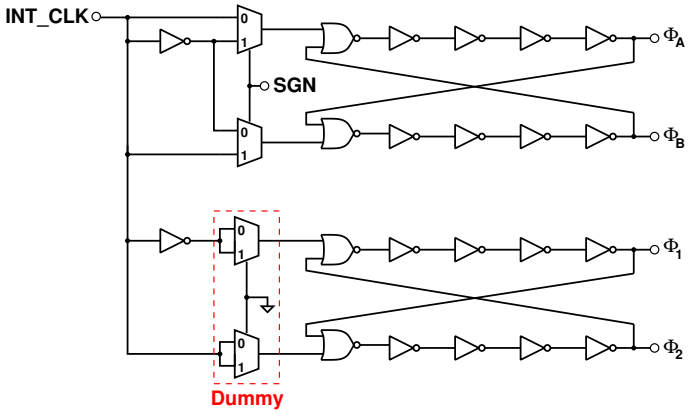

Figure 6. Circuit schematic of the non-overlapping phase generator (bottom) and the phase-swapping generator (top) for the switched-capacitor integrator.

3.3. Digital Control Unit (DCU)

The core architecture of the DCU is depicted in Figure 7. The circuit includes three Galois LFSR registers [5], namely LFSR1, LFSR2, and LFSR3; an OR logic port; and a

multiplexer. These registers have the option to load a start state through the INIT input buses. The loading is triggered by the LOAD input signal (active high). Additionally, they have an internal logic that is able to set the CNT output signal to 1 as the MLS is completed. The LOAD inputs of both LFSR1 and LFSR2 are connected to the global RESET of the DCU. The CNT output of LFSR1, SAMPLE_RDY, is used as a clock signal for LFSR2. STATE[0] and STATE[1] are pre-computed digital words and are the first and second states, respectively, of the LFSRs. The circuit's operation is explained with reference to the simplified case of a 3-bit (N equal to 7) LFSR seen in Figure 8.

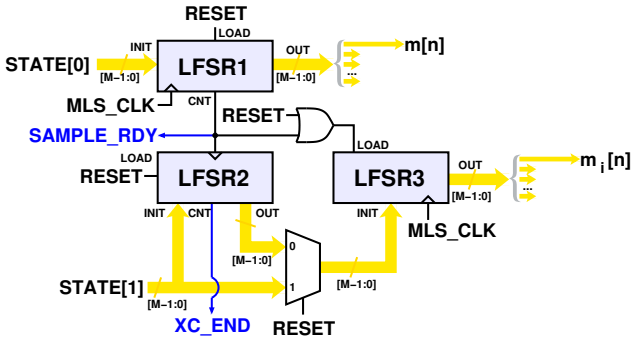

Figure 7. Circuit schematic of the digital control unit (DCU) for the generation of MLS sequences.

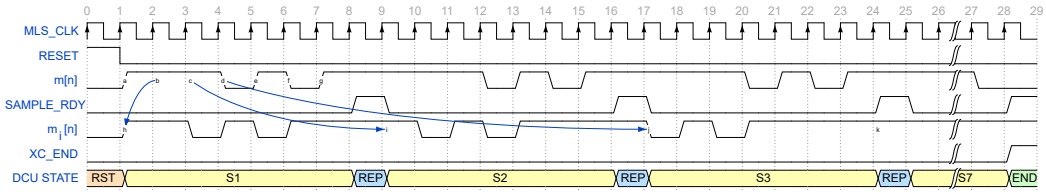

Figure 8. Waveform diagram of the DCU signals by considering an L equal to 3 (N equal to 7).

As the global RESET signal is asserted (0th cycle), LFSR1 and LFSR2 load the STATE[0] and STATE[1] words, respectively. LFSR3 loads the STATE[1] word since its LOAD input, i.e., the output of the OR port is set to 1 and the "1" input of the multiplexer is selected. During the first complete sequence (S1 state from the first to the seventh cycles), LFSR1 and LFSR3 produce exactly the same MLS sequence but the starting index of LFSR3 is incremented by 1 with respect to LFSR1. As LFSR1 and LFSR3 end their sequences (eighth cycle), their CNT outputs go high for a clock cycle (see SAMPLE_RDY at the eighth cycle). This output signals the end of the current sequence. During this clock cycle, the states of $\mathbf{m}$ and $\mathbf{m}_i$ are repeated. Since the SAMPLE_RDY output serves as the clock input for LFSR2 at its positive edge, the state of LFSR2 accomplishes a step forward and becomes S2. Since the "0" input of the multiplexer is selected (the RESET signal is 0) and since the LOAD input of LFSR3 is 1, the LFSR3 initial state for the new sequence is incremented to S2. As a result, the starting index of the $\mathbf{m}_i$ sequence will be incremented at every $\mathbf{m}$ completion (see the 9th and 17th cycles). The algorithm ends after seven repetitions during which the whole 7×7 $\boldsymbol{C}$ circulant matrix has been serially provided at the $\mathbf{m}_i$ output. The end of the operation is signaled through the CNT output of LFSR2 (see XC_END at the 29th cycle).

A conventional way to accomplish the $\boldsymbol{C}$ matrix in integrated digital circuits is actually to hard-code the matrix content in a circuit made of tie cells. This solution works for very small matrices but fails as the required size increases. A more efficient solution is the adoption of a dedicated ROM memory but it could have a big area for large matrices. Moreover, the ROM size increases, as multiple $\boldsymbol{C}$ matrices of different M orders are required.

Multiple DCUs, each of a different LFSR order, M, were designed. As depicted in Figure 9, the implemented bit orders are 5 bit (only for test purposes), 8 bit, 10 bit, 12 bit, and 14 bit. Depending on the application, the user can choose the desired M order through the M_SEL signals.

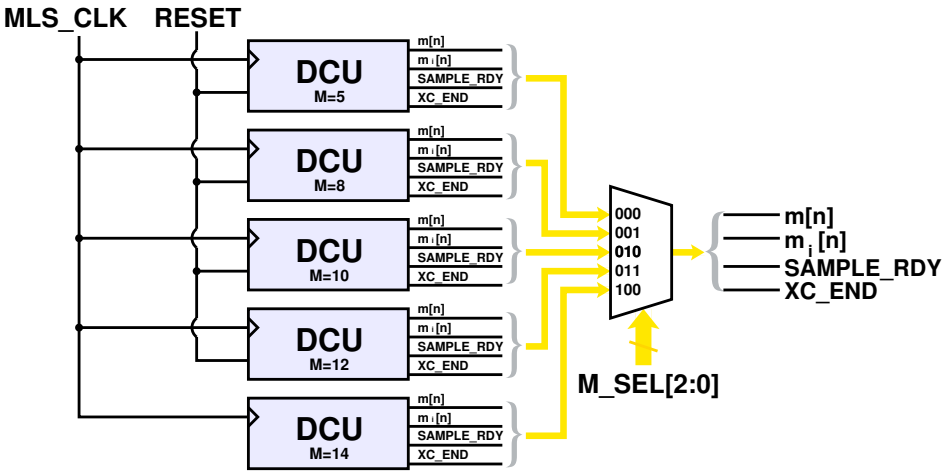

Figure 9. Circuit schematic of the implemented selectable DCU.

3.4. Noise Estimation

Electronic noise plays a role in degrading the accuracy of the $\mathbf{h_z}$ samples resulting from the analog cross-correlation operation. Only the thermal noise is considered since the effect of the flicker noise is assumed to be removed thanks to the implemented CDS technique implemented in the integrator [15–17]. The analytical expression of the integrated thermal noise at the system's output, $V_{\Phi n}$, can be derived by considering two main contributions: the noise from the AFE and the noise from the integrator. The first is calculated with reference to Figure 3 as follows:

$$\overline{v_{no,AFE}}^2 \approxeq \gamma \cdot \frac{kT}{C_S} \cdot R_S \cdot g_{m4,5} \tag{15}$$

where γ is the noise factor considered to be equal to 2/3, R_S and C_S are the electrical parameters of the sensor's simplified model, and $g_{m4,5}$ is the small-signal transconductance of both the M4 and M5 MOSFETs in Figure 3. The latter was found to be very similar for both the M4 and M5 MOSFETs and it was determined through SPECTRE simulation to be about 200 µS. Regarding the contribution from the CDS integrator, an approximate expression for its input-referred noise can be found in [16]:

$$\overline{v_{no,INT}}^2 \approxeq \frac{4\,kT}{OSR \cdot C_S} \cdot 2 \tag{16}$$

where C_S is the sampling capacitor and the OSR is the oversampling ratio, whose value is, in this case, equal to the ratio between the integrator's sampling frequency, f_m, and the sampling frequency of the external ADC, which is f_m/N. The approximate expression of the output-referred noise of the entire system, $V_{\Phi n}$, is derived as follows:

$$\overline{v_{\Phi n}}^2 \approxeq kT \cdot \left|\frac{C_S}{C_F}\right|^2 \cdot \left(\frac{8}{N \cdot C_S} + \frac{\gamma \cdot R_{sens} \cdot g_{m4,5}}{C_{sens}}\right) \tag{17}$$

Equation (17) proved to be useful for a first-order evaluation of the accuracy of the entire system.

4. Simulation Results

The single blocks shown in Figure 2 were simulated and verified in the Cadence Virtuoso Platform through a SPECTRE simulation. However, the long time required for a complete cross-correlation simulation did not permit a transistor-level verification of the entire system. Thus, the AFE and integrator were modeled using transistor-level specifications with the Verilog-A models. In this way, it was possible to verify the correctness of the circuit's operation.

Figure 10 depicts the waveforms from the simulation. In particular, a simple parallel RC circuit was used as the test impedance with an 8-bit MLS input signal and a sampling frequency, f_m, of 1 MHz. The latter limited the maximum detectable bandwidth to 500 kHz. The sensor's electrical components were chosen as 50 kΩ and 100 pF for the resistance and capacitance, respectively. The MLS current amplitude, $|I_m|$, was set to 10 µA, as mentioned in Section 3.1. Regarding the integrator, the 30 pF value was selected from the variable capacitor seen in Figure 11 (S0, S1, S2, S3 inputs with low values), leading to an integration gain of 0.0167. The output voltage from the SPECTRE simulation was compared with that from the ideal MATLAB model in Figure 12.

Figure 13 shows the discrete-time analog cross-correlation from the SPECTRE simulation. As can be seen, the integrator's output voltage (blue curve) was sampled by the external ADC to generate the cross-correlation samples (red curve). A detail of the cross-correlation operation is depicted in Figure 14. As derived in Section 2, the discretized time-domain impedance of the sensor, $h_z[n]$, was obtained by multiplying the sampled version of the integrator's output voltage (red curve in Figure 13) by the ψ scaling factor introduced in (9).

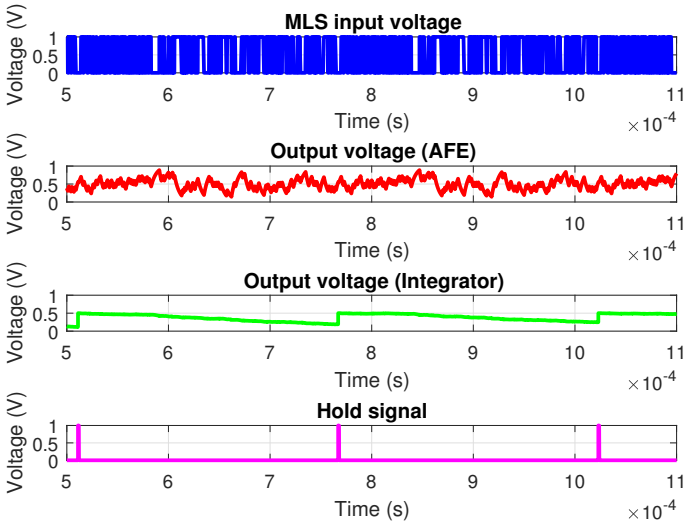

Figure 10. Waveforms from SPECTRE simulation.

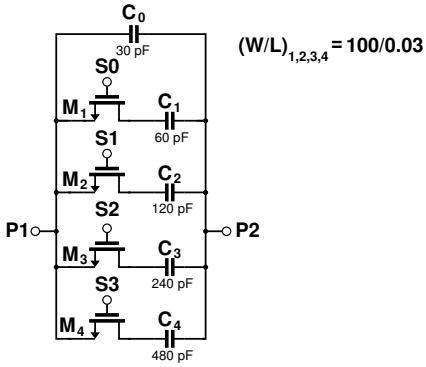

Figure 11. Circuit schematic of the variable capacitor C_F. The specified width/length are reported in µm for each MOSFET.

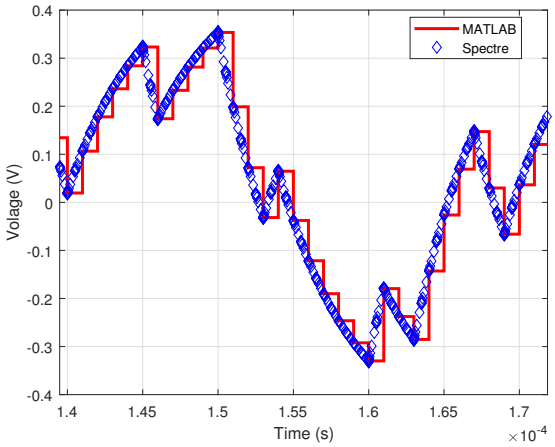

Figure 12. Comparison of AFE output voltages from theoretical (MATLAB) and circuit-level (SPECTRE) simulations.

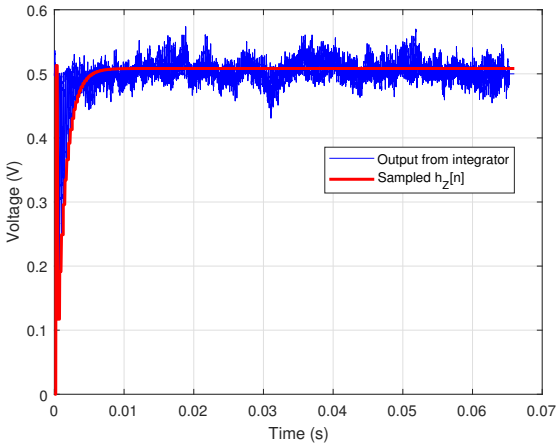

Figure 13. Integrator's output voltage (blue curve) and its sampled replica (red curve).

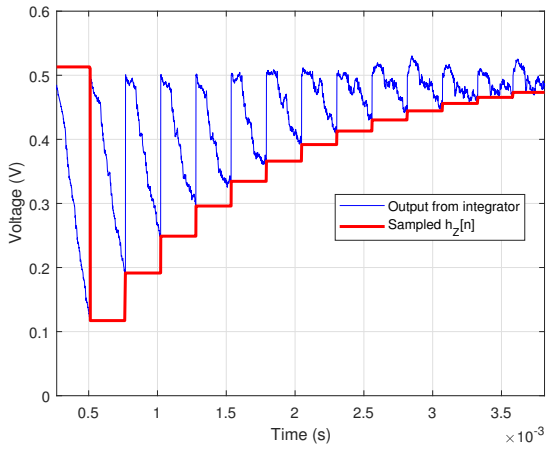

Figure 14. Detail of the cross-correlation operation.

In Figure 15, the theoretical $\mathbf{h_z}$ curve (green) is compared with the simulated results obtained from the MATLAB (red points) and SPECTRE (blue points) implementations, showing good agreement between them.

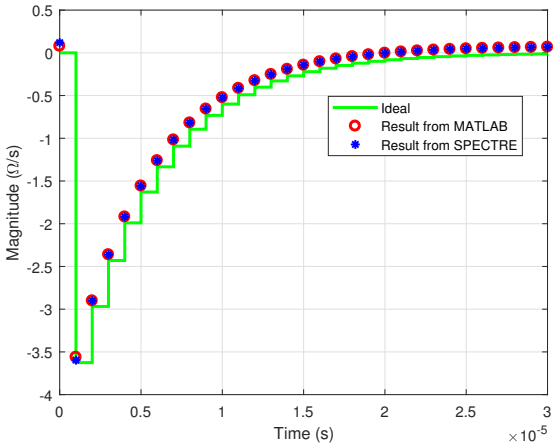

Figure 15. Theoretical time-based EIS (green curve) compared with simulation results from MATLAB (red points) and SPECTRE (blue points) implementations, respectively.

The thermal noise effect which, as also mentioned, impacts the system's accuracy, was modeled in the simulation environment. Its effect can be observed in Figure 16, in particular, in the right portion of the curve. The criterion introduced in [5] was used here for the direct extraction of the SNR from the simulated output curve. Briefly, the time-based impedance was divided into two portions using the crossing of the curve on the X axis, i.e., the zero crossing point, as the discriminant index. In the left portion, the signal contribution was prevalent with respect to the noise, whereas in the right portion, the noise contribution was prevalent with respect to the signal. Thus, the signal power, P_S, was computed through the following equation:

$$P_S = \frac{1}{N} \cdot \sum_{n=0}^{i} \left| \frac{V_\Phi[n]}{\psi} \right|^2 \tag{18}$$

where i is the zero-crossing index. Regarding the noise power, P_N, it was computed by calculating the variance of the right portion by assuming a Gaussian distribution of the noise sources. As a result, a simulated SNR of 75 dB was obtained for the specific modeled sensor.

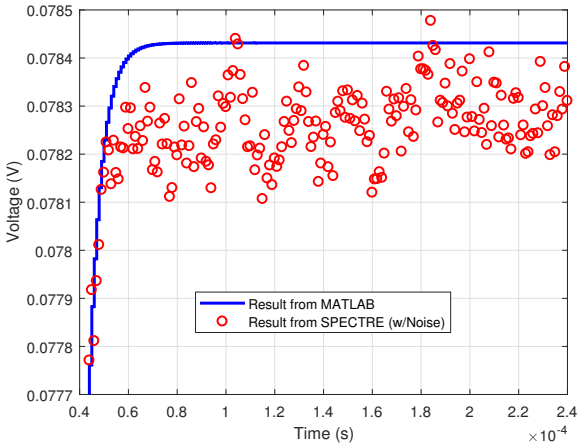

Figure 16. Ideal output from MATLAB implementation (blue curve) compared with output from SPECTRE (red points) in presence of thermal noise.

This value differed from the theoretical value obtained by considering only the thermal noise power derived in (17) in the SNR calculation. By substituting the values in the equation, a theoretical SNR of 100 dB was obtained. The discrepancy between the simulated and theoretical SNR can be explained by considering that the latter only took into account

the thermal noise from the circuit, whereas the former also contemplated the precision error of the sensor's initial condition. Indeed, the error voltage in the V_{ic} voltage (see Figure 3) translated to a cross-correlation error which, in turn, impacted as an error in the discrete-time impedance of the sensor. Regarding the power consumption, a value of 420 µW was obtained from the simulation. In (12), the measurement time was equal to 65 ms for the considered test impedance and the used MLS frequency of 1 MHz. The energy-per-measurement (EpM) value was obtained by multiplying the power consumption by the measurement time, resulting in 27.4 µJ for the simulated circuit.

Figure 17 shows the layout of the chip with an emphasis on the analog and mixed-signal core. The latter measures about 0.034 mm^2.

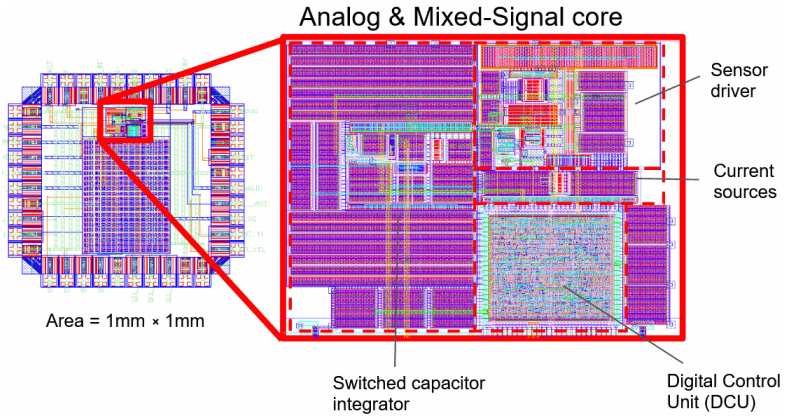

Figure 17. Chip layout.

Table 2 shows a performance comparison with state-of-the-art integrated systems for EIS. The max detected error of the presented work is comparable with [10]. However, it can be noted that although in [10] the error is taken from the absolute maximum INL over the measured frequency range, in the proposed work, it is obtained from the SNR of the entire simulated curve. In particular, the SNR is converted to an RMS error by considering the measurement error as a Gaussian noise signal referred to as a 1 V RMS amplitude sinusoidal signal. Thus, the specified error takes into account the error of the entire curve. The obtained RMS error is 0.0177%, which corresponds to 177 ppm. Although the error is comparable with those of state-of-the-art systems, the proposed solution exhibits the best performance in terms of power consumption per measured points. The number of measurable points can be increased up to $2^{14} - 1$.

Table 2. Comparison with state-of-the-art systems.

	[10]	[9]	[6]	[18]	**This Work**
Approach	Frequency-based (ΔΣ demodulation)	Frequency-based (magnitude/real part measurement)	Frequency-based (magnitude/phase measurement)	Frequency-based (MLS/DMLS + read-out, DSP not included)	Time-based (MLS + analog cross-correlation)
CMOS Process	0.35 µm	180 nm	0.35 µm	180 nm	28 nm FD-SOI
Chip area	9 mm^2	N/A	0.4 mm^2	N/A	0.034 mm^2 (core)
Tested impedance	68 Ω ‖ 1 µF	200 Ω + (5 kΩ ‖ 45 nF)	Equivalent circuit of the electrode/tissue impedance	100 Ω ‖ (100 Ω + 220 nF)	50 kΩ ‖ 100 pF
Stimulus generator	Yes	No	No	Yes	Yes
Max tested frequency	16 kHz	1 MHz	100 kHz	125 kHz	500 kHz (capable of measuring up to 50 MHz)
Measured points	1	1	1	63	255 (capable of measuring up to 2^{14} points)
Max Error	0.0166 % (INL)	0.3% (magnitude error, simulated)	1.15% (magnitude error)	>10% (resistor error)	0.0177 % (RMS on entire curve, simulated)
Max power consumption	5.8 mW	0.513 mW	21 mW	0.155 mW	0.420 mW

5. Conclusions

In this paper, an integrated circuit for the time-based measurement of sensors' impedance has been presented. The circuit exploits the impulse response measurement concept through the use of maximum-length sequences and a cross-correlation operation. Unlike the conventional approach, the proposed solution implements the cross-correlation in the analog domain. This allows the analog-to-digital conversion to be moved after the signal processing, leading to several benefits: (1) the measured time-based impedance is not affected by the ADC's quantization noise, thus increasing measurement accuracy; (2) the sampling rate of the ADC is greatly relaxed since only the last cross-correlation sample is converted, thus reducing the system's complexity; and (3) RAM usage is avoided, thus reducing efforts in digital design. Theoretical concepts about the circuit's design and operation were presented with consideration of the thermal noise phenomenon. The simulated performances were shown by testing a sensor's equivalent model composed of a 50 kΩ resistor in parallel with a 100 pF capacitor. A time-based output impedance of 255 points was obtained with a maximum tested frequency of 500 kHz and a simulated RMS error of 0.0177% (or 177 ppm).

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Abbreviations

The following abbreviations are used in this manuscript:

ADC	analog-to-digital converter
AFE	analog front end
CMOS	complementary metal-oxide semiconductor
DCU	digital control unit
EIS	electrical impedance spectroscopy
EpM	energy per measurement
FD-SOI	fully depleted silicon on insulator
GBW	gain-bandwidth product
IR	impulse response
LFSR	linear feedback shift register
LTI	linear time-invariant
MLS	maximum-length sequence
MOSFET	metal-oxide-semiconductor field-effect transistor
MOX	metal oxide
PM	phase margin
PRBS	pseudo-random binary sequence
RAM	random access memory
SNR	signal-to-noise ratio
SUT	sensor under test

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